19.7 A Multi-Stage Interleaved Synchronous Buck Converter with Integrated Output Filter in a 0.18μm SiGe Process

Siamak Abedinpour[1], Bertan Bakkaloglu[2], and Sayfe Kiaei[2]

[1]Freescale Semiconductor, Tempe, AZ
[2]Arizona State University, Tempe, AZ

State-of-the-art mobile terminals utilize a multi-output centralized power management unit with external filter inductors and capacitors that powers various sections through multiple I/O pads and PCB interconnects. This introduces significant system noise, delay, and power loss. In this paper a fully integrated switched-mode (SM) step-down dc-dc converter as a main building block of a monolithic distributed power management architecture is presented. The fully-integrated converter provides a programmable 1.5 to 2V output voltage with 200mA current rating with a monolithic output *LC* filter. The converter is designed and fabricated in 0.18μm SiGe RFBiCMOS process technology and achieves a switching frequency of 45MHz at nominal load conditions.

Implementation of high switching frequency, multi-phase interleaved topology, and a fast hysteretic controller has reduced the filter inductor and capacitor sizes by two orders of magnitude compared to state-of-the-art converters, and enabled a fully integrated converter. However, switching losses are directly proportional to the converter switching frequency, and this imposes a limit on high-frequency operation of SM dc-dc converters. In this design, a zero-voltage switching (ZVS) synchronous buck converter topology is implemented, where the voltage across the power device terminal is zero during the switching transient, minimizing the switching losses and improving the efficiency of the converter [1]. To our knowledge this is the first reported fully integrated multi-stage interleaved ZVS synchronous buck converter with monolithic output filters.

For efficient ZVS operation it is desirable to achieve a peak-to-peak current ripple equivalent to twice the full load current. The inductor value L_f that guarantees this peak-to-peak current ripple is given by Equation (1), where D is the steady-state duty cycle, f_s is the switching frequency, and I_o is the nominal output current.

$$L_f \leq \frac{(V_{in} - V_{out})D}{2f_S I_o} \quad (1)$$

Although a smaller inductor value enables a faster transient response, it also results in larger current ripple, which causes higher conduction losses in the switches, inductor, and parasitic resistances. The smaller inductor also requires a larger filter capacitor to decrease the output voltage ripple. In order to maintain low steady-state output voltage ripple and fast transient response, N similar stages of converters can be operated in parallel with a common output filter capacitance. By applying a $360^\circ/N$ phase difference between the triggering pulses of the adjacent power stages, the output current ripple can be cancelled out while maintaining the fast transient response characteristics of a single stage [2]. Multiple filter paths and switching pairs also improve the thermal distribution and reliability of the integrated converter. The output current ripple cancellation depends on N and D, and improves with more modules in parallel. In this design, a two-stage interleaved converter has been implemented, where the ripple can be ideally cancelled when $D = 0.5$, and reduced at other values of D.

Figure 19.7.1 shows the circuit diagram of the implemented two-stage interleaved ZVS synchronous buck converter. The integrated output filter and high efficiency multi-stage ZVS operation are the main differentiators between this design and previously reported converters [3]. Figure 19.7.2 shows the gate pulse waveforms of M_1 and M_3, the current through the filter inductors L_{f1} and L_{f2}, the output current i_o, the filter capacitor current i_c, and the output load current I_o. A current-mode comparator compares the converter output voltage, V_{out}, with the reference signal V_{ref} and generates the *PWM* signal at its output. The *PWM* signal is applied to a phase-shift block, which generates the PWM_1 and PWM_2 signals with a 180° phase difference. These signals are then applied to the ZVS controller blocks to generate the gate control pulses φ_1-φ_4 to control the switching of power MOSFETs M_1-M_4. The ZVS controller consists of two separate gate drive circuits for the PMOS and NMOS power switches and a logic circuit to ensure precise non-overlap time between two pulses. The $PWM_{1,2}$ signals are applied to the logic circuit, which uses the $\varphi_{1,3}$ and $\varphi_{2,4}$ pulses from the output of the gate drive circuits as feedback signals to introduce a dead-time between the PWM_n and PWM_p pulses. These signals are then applied to the gate drive blocks and generate the $\varphi_{1,3}$ and $\varphi_{2,4}$ pulses to be applied to the converter power MOSFETs. The PMOS gate drive circuit uses a cascade of five inverters, and NMOS uses four inverter stages to generate control pulses driving the large gate capacitance of the power MOSFETs. A scaling factor of 5 is chosen between inverter stages in order to optimize propagation delay and minimize dynamic power loss.

The power train of the converters consists of M_1-M_4, and the filter inductors and capacitors. M_1-M_4 are implemented with 3.3V MOSFETs with 70A° gate-oxide thickness. The device widths $W_{n,p}$, are optimized by equating the conduction and switching losses of the switches, minimizing their total power loss. M_1-M_4 are formed by a parallel connection of an array of unit-size cells, which have a width of 20μm, and multiple gate-fingers with a minimum gate length of 0.5μm. The widths of the unit-size cells are optimized in order to reduce the *RC* delay due to the gate structures, which affects the switch transitions.

The integrated filter capacitor C_f = 6nF is built by a parallel array of 1pF unit-size cells. The gate capacitor in this process provides a specific capacitance of 8fF/μm². In order to obtain a high-performance inductor, L_f = 11nH, a patterned 10μm thick electroplated copper layer is utilized. However the inductor conduction loss is still the dominant factor in determining the integrated converter efficiency.

Figure 19.7.3 shows the measured output waveform of the two-stage interleaved ZVS synchronous buck converter portion of the chip. Fully integrated filter components are designed for a nominal switching frequency of 100MHz. As the gate drive parasitics and propagation delays in the feedback loop increase, the converter switching frequency may reduce, increasing output ripple. Figure 19.7.4 and Fig. 19.7.5 show the efficiency variation of single-stage and two-stage synchronous and ZVS synchronous buck converters versus load current. Figure 19.7.6 shows the transient response of the two-stage interleaved converter to a step load of 50mA. The load regulation is <3%. Figure 19.7.7 shows the micrograph of the IC with fully integrated converters. The two-stage interleaved converter occupies a silicon area of 3mm×9mm.

References:

[1] D. Maksimovic, "Design of Zero-Voltage Switching Quasi-Square-Wave Resonant Switch," in *Proc. IEEE Power Electronics Specialists Conference*, pp. 323-329, June, 1993.

[2] X. Zhou et al., "Investigation of Candidate VRM Topologies for Future Microprocessors," *IEEE T. Power Electronics*, vol. 15, no. 6, pp. 1172-1182, 1993.

[3] P. Hazucha et al., "A 233 MHz 80%-87% Efficient Four-Phase DC-DC Converter Utilizing Air-Core Inductors on Package," *IEEE J. Solid-State Circuits,* vol. 40, no. 4, pp. 838-845, 2005.

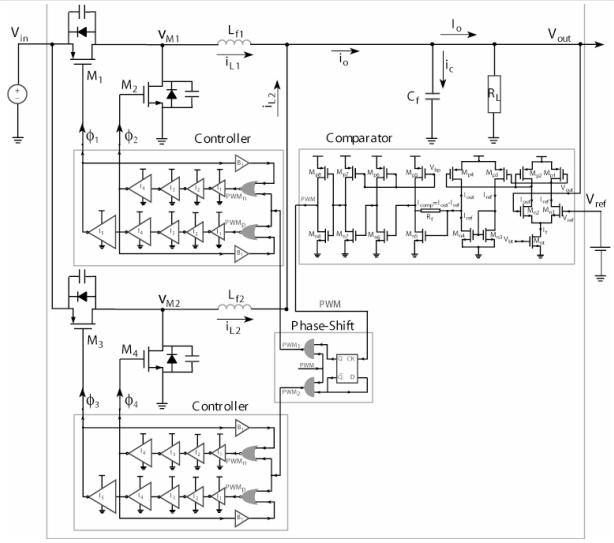

Figure 19.7.1: Circuit diagram of the fully integrated two-stage interleaved ZVS synchronous buck dc-dc converter.

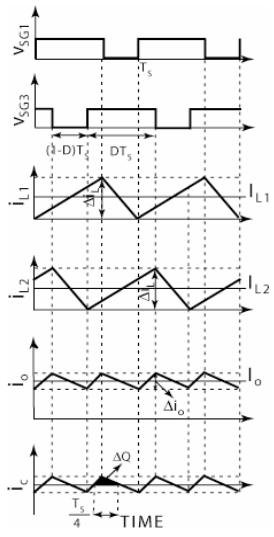

Figure 19.7.2: Timing diagrams associated with two-stage interleaved ZVS synchronous buck dc-dc converter.

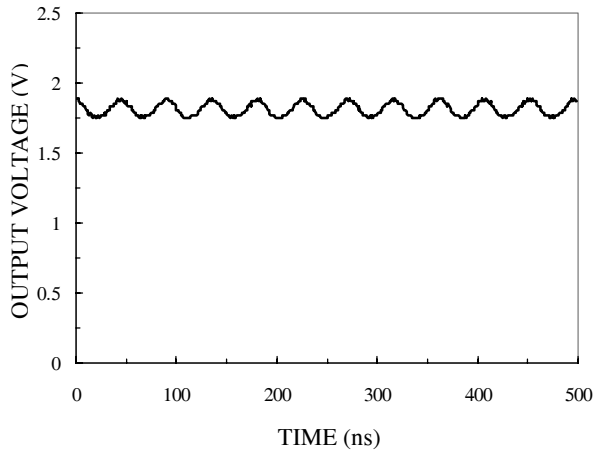

Figure 19.7.3: Measured output waveform of the two-stage interleaved ZVS synchronous buck converter for V_{in}= 2.8V, V_{out}= 1.8V, with a resistive load of 22Ω.

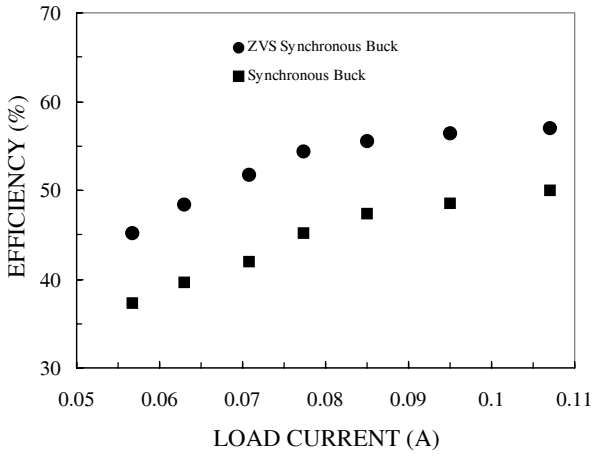

Figure 19.7.4: Efficiency versus load current for single-stage synchronous buckand ZVS synchronous buck converters, for V_{in}= 2.8V and V_{out}= 1.8V.

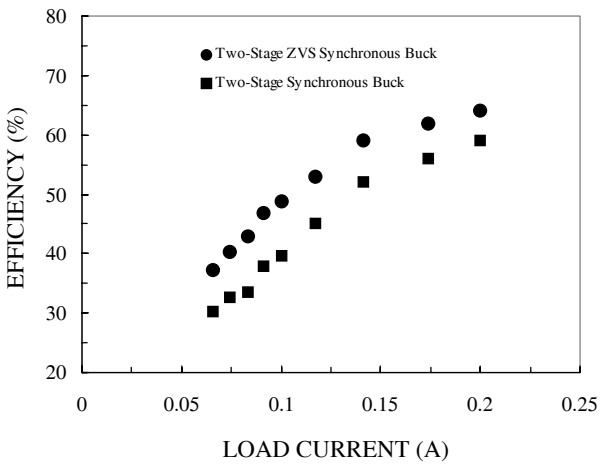

Figure 19.7.5: Efficiency versus load current for two-stage interleaved and two-stage interleaved ZVS synchronous buck converters, for V_{in}= 2.8V and V_{out}= 1.8V.

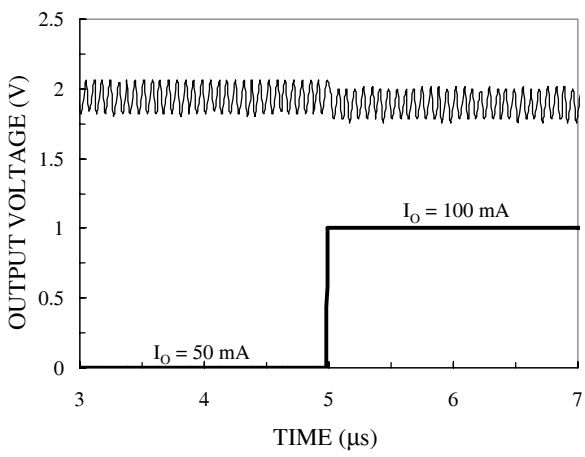

Figure 19.7.6: Transient response of the two-stage interleaved ZVS synchronous buck converter to a step load of 50mA at V_{in}= 2.8V and V_{out}= 1.9V.

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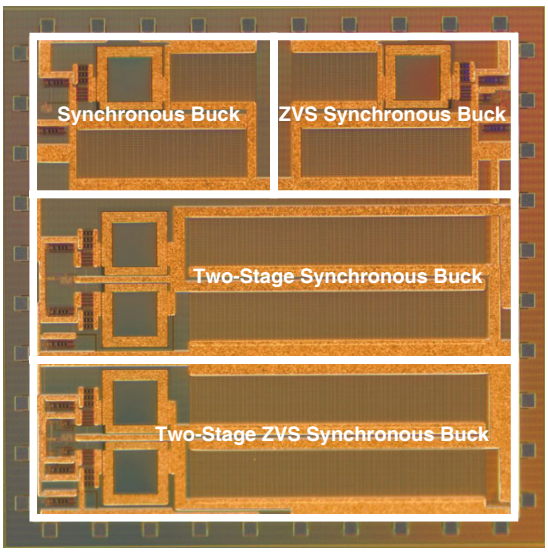

Figure 19.7.7: Die micrograph.

